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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,872	02/26/2002	Joseph A. Iadanza	BUR920010100	6213

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SCHMEISER, OLSEN + WATTS
SUITE 201
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LATHAM, NY 12033

EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,872	IADANZA, JOSEPH A.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-28* is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Remarks, filed September 9, 2004, with respect to the rejection(s)of claim(s) 1-16 under 35 U.S.C. 102 (e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as show below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, as disclosed on figures 1-2 and their description in the instant application in view of Bohr (U.S. Patent No. 6,617,681). With regard to Claim 1, Applicant's admitted prior art discloses (see figure 1) a predefined block of functional circuitry (160) having a plurality of I/O pins (175).

Applicant's admitted prior art fails to disclose a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit. However, Bohr discloses a backside I/O pad (224) electrically connected to a backside via of an integrated circuit structure (see figure

15). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die to a substrate (column 12, lines 35-37).

With regard to Claim 2, Applicant's admitted prior art discloses I/O pins (175) formed in a lower interconnect level of an integrated circuit chip (see figure 1).

With regard to Claim 3, Applicant's admitted prior art discloses I/O pins (175) formed in a lowest interconnect level of an integrated circuit chip (see figure 1).

With regard to Claim 4, Applicant's admitted prior art discloses an integrated circuit fabricated using a bulk silicon substrate or using a silicon-on-insulator substrate (see paragraph 0004, line 2).

With regard to Claim 5, Applicant's admitted prior art predefined block of functional Circuitry (160) includes a first portion containing functional circuitry (165) and a second portion (170) containing said I/O pins (175), (see figure 1).

With regard to Claim 6, a further difference between Applicant's admitted prior art and the claimed invention is, a backside via connected to the second portion. Bohr discloses a backside

I/O pad (224) electrically connected to a backside via of an integrated circuit structure (see figure 15). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed a backside via connected to the second portion, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die to a substrate (column 12, lines 35-37).

With regard to Claim 7, Applicant's admitted prior art discloses a plurality of front-side I/O pads (150) and additional I/O pins contained in metallization layer (130), each additional I/O pin electrically connected to one front-side I/O pad of the integrated circuit by a global wiring connection (see figure 1).

With regard to Claim 8, Applicant's admitted prior art discloses non-predefined circuitry (see figure 1), which is circuitry other than that contained in core region (160).

With regard to Claim 9, Applicant's admitted prior art discloses a plurality of front-side I/O pads (150) and non-predefined circuitry having a plurality of I/O pins contained in metallization layer (135), each additional I/O pin electrically connected to one front-side I/O pad of the integrated circuit by a global wiring connection (see figure 1).

With regard to Claim 10, Applicant's admitted prior art discloses additional predefined circuitry having a plurality of I/O pins contained in metallization layer (140), each additional I/O pin

electrically connected to one front-side I/O pad of the integrated circuit by a global wiring connection (see figure 1).

With regard to Claim 11, Applicant's admitted prior art discloses providing a predefined block of functional circuitry (160) having a plurality of I/O pins (175).

Applicant's admitted prior art fails to disclose connecting a backside I/O pad electrically to each I/O pin through a backside via of the integrated circuit. However, Bohr discloses a backside I/O pad (224) electrically connected to a backside via of an integrated circuit structure (see figure 15). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include connecting a backside I/O pad electrically to each I/O pin through a backside via of the integrated circuit, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die to a substrate (column 12, lines 35-37).

With regard to Claim 12, Applicant's admitted prior art discloses providing additional I/O pins contained in metallization layer (145), electrically connecting each additional I/O pin to one front-side I/O pads (150) of the integrated circuit by a global wiring connection (see figure 1).

With regard to Claim 13, Applicant's admitted prior art discloses providing a non-predefined circuitry (see figure 1), which is circuitry other than that contained in core region (160).

With regard to Claim 14, Applicant's admitted prior art discloses a plurality of front-side I/O pads (150) and additional I/O pins contained in metallization layer (130), each additional I/O pin electrically connected to one front-side I/O pad of the integrated circuit by a global wiring connection (see figure 1).

With regard to Claim 15, Applicant's admitted prior art discloses additional predefined circuitry having a plurality of I/O pins contained in metallization layer (140), each additional I/O pin electrically connected to one front-side I/O pad of the integrated circuit by a global wiring connection (see figure 1).

With regard to Claim 16, a further difference between Applicant's admitted prior art and the claimed invention is, a backside via connected to the second portion. Bohr discloses a backside I/O pad (224) electrically connected to a backside via of an integrated circuit structure (see figure 15). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed a backside via connected to the second portion, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die to a substrate (column 12, lines 35-37).

Allowable Subject Matter

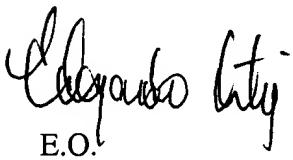
3. Claims 23-28 are allowed.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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